

## Interface Characterization in III-V CMOS Nanoelectronics

L.V. Goncharova<sup>a</sup>, O. Celik<sup>b</sup>, T. Gustafsson<sup>a</sup>, E. Garfunkel<sup>b</sup>, M. Warusawithana<sup>c</sup>, D.G. Schlom<sup>c</sup>, H. Wen<sup>d</sup>, M.B. Santos<sup>d</sup>, Safak Sayan<sup>e</sup>, Wilman Tsai<sup>e</sup> and Niti Goel<sup>e</sup>

<sup>a</sup> Department of Physics, Rutgers University, Piscataway, New Jersey 08854, USA

<sup>b</sup> Department of Chemistry, Rutgers University, Piscataway, New Jersey 08854, USA

<sup>c</sup> Department of Materials Science and Engineering, Penn State University, University Park, PA 16802 USA

<sup>d</sup> Homer L. Dodge Department of Physics and Astronomy, University of Oklahoma, Norman 73019

<sup>e</sup> Intel Corporation, Santa Clara, CA, 95952

A central requirement in the integration of III-V substrates in highly scaled CMOS gate stacks is to develop an ability to assure that we create a high capacitance, high mobility transistor structure with a low concentration of defects. In this contribution, recent studies of the compositional profile and interdiffusion of high-K gate stacks on III-V substrates are reviewed. Sulfur passivation methods have been explored to help ensure that the starting III-V surface (InGaAs in this case) has a low defect concentration. Diffusion processes associated with the introduction of oxygen-gettering metal gate materials will also be discussed.

### Introduction

The semiconductor industry is considering the use of III-V materials for post-silicon CMOS transistor channels. III-V semiconductor intrinsic characteristics – high electron mobility, high breakdown fields, semi-insulating substrate - will lead in the future to high-speed devices and will offer high power applications. Interface passivation and defect issues remain central to the viability of this attempt at integration. After several decades of research, a few interfaces with dielectric oxides has been developed that show promising results: molecular beam deposition of Ga<sub>2</sub>O<sub>3</sub>-Gd<sub>2</sub>O<sub>3</sub> mixtures or Gd<sub>2</sub>O<sub>3</sub>, (1) atomic layer deposition of Al<sub>2</sub>O<sub>3</sub>, (2) thin passivation InP layers, (3) an amorphous Si interface passivation layer, (4) and S passivation (5) (prior to further film deposition). The interfacial layer thickness and composition, and the device properties, are strongly effected by the surface preparation, growth chemistry, thermal treatment and nature of the metal gate.

In this study we present results from two sets of high-k dielectric films grown on InGaAs. A schematic diagram of two film structures that we have grown is shown in Fig. 1. We have explored both low and high In concentration substrates, with In/(In+As) ratios of between ~0.1-0.5. The epitaxial InGaAs layer is thick enough that there should be no chemical or electrical effect of the substrate GaAs layer located several tens to hundreds of nm away. We have grown several different oxides on InGaAs, including HfO<sub>2</sub> and LaAlO<sub>3</sub> presented here. We have used S passivation methods on the InGaAs substrate prior to high-K deposition, and in the work reported here, determine the stability of the S-containing layer. In addition, full analysis of the elemental depth

profiles of this film structures yields some indication of interfacial layer formation and interdiffusion between the layers.

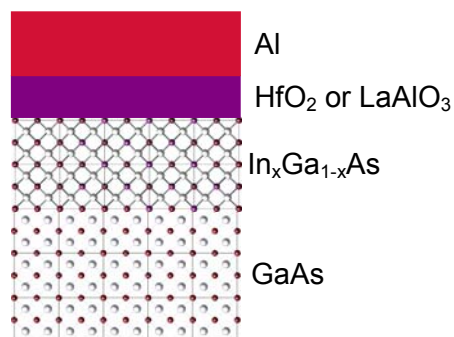


Fig. 1 Simplified schematic of an ideal gate stack with an epitaxial InGaAs channel, an amorphous high-K dielectric ( $\text{HfO}_2$  or  $\text{LaAlO}_3$ ), and a metal electrode.

### Experimental

We have examined a series of different III-V gate stack structures before and after passivation, high-K growth, and gate metallization. The top channel InGaAs layers were deposited using ultra-high vacuum molecular beam epitaxy (MBE) on (i) GaAs(001) for  $x = 0.10$ - $0.15$   $\text{In}_x\text{Ga}_{1-x}\text{As}$ , and (ii) InP (001) for a 52% doped  $\text{In}_x\text{Ga}_{1-x}\text{As}$  layer. After channel layer growth, the surface of some samples were passivated with sulfur, following procedures described in the literature,<sup>(5, 6)</sup> while others were made by atomic layer deposition ( $\text{HfO}_2$ ) or MBE ( $\text{LaAlO}_3$ ) using dry  $\text{N}_2$  cleaning prior to deposition of the amorphous dielectric film. Although scanning probe microscopy (SPM) results are not included here, we do note that UHV SPM studies (taken with an Omicron VT-SPM system) show that roughening can be a problem when etching the III-V substrates during cleaning and sulfur passivation.

Our experimental toolset has included medium energy ion scattering (MEIS), x-ray photoelectron spectroscopy (XPS) and SPM. MEIS is a low energy, high resolution variant of Rutherford backscattering spectroscopy. The technique is quantitative, as scattering cross sections are known accurately for the energies ( $\sim 100$ - $130$  keV) and projectiles (protons) we use. The backscattered ions were detected by a toroidal electrostatic ion energy analyzer and were corrected for neutralization effects. In order to reduce the background in the spectra, double alignment scattering geometries (7, 8) were used. Photoelectron spectra were taken with a conventional XPS system, using Mg  $K\alpha$  radiation.

### Results

We first show MEIS results and focus on the interaction of S in the passivation layer with the substrate, dielectric and metal electrode. Initial effects of the S passivation procedure include removing of the native oxide layer and formation of 2-5Å thick sulfide. Under certain passivation conditions, InGaAs surface roughening also occurs during the etching procedure. Although it might have been expected that S, being more weakly bound than O, would be removed from the system during dielectric growth, our results do not show this. The MEIS spectra were modeled and clearly showed that S is present in

the system at a 1-2ML level after dielectric growth (Fig. 2). When the dielectric is grown, the S incorporates first in the dielectric, close to the dielectric/semiconductor interface. From a thermodynamic perspective this is not unexpected. Although S bonds to the metal and semiconductor more weakly than O, with metal and/or semiconductor present in excess, the S can readily incorporate into the film rather than “float” on top as a surfactant.

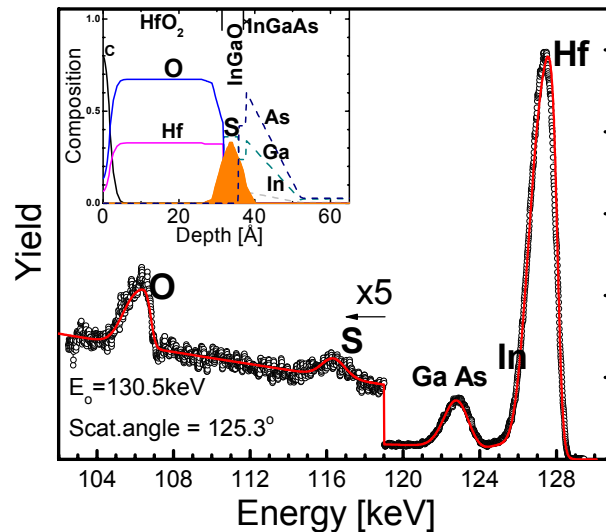


Fig. 2. MEIS spectrum of a  $\text{HfO}_2/\text{S}/\text{InGaAs}$  stack. The red line through the spectrum is a fit to a model multilayer structure.

#### Interface behavior in the $\text{LaAlO}_3/\text{InGaAs}$ system

Since promising thermal stability and  $>1\text{eV}$  band offset were observed in molecular beam deposited amorphous  $\text{LaAlO}_3/\text{Si}$  structures,<sup>(9)</sup> we explored the possibility of integrating  $\text{LaAlO}_3$  with  $\text{InGaAs}$ . A sharp interface was achieved for an amorphous  $\text{LaAlO}_3$  film grown by MBE on  $\text{InGaAs}$ . Fig. 3 shows MEIS spectra with separate oxygen, aluminum, gallium/arsenic, and lanthanum/indium peaks. By simulating the spectra, we conclude that they are, within the 0.2 - 0.3 nm resolution of this analysis, consistent with an abrupt interface between the  $\text{LaAlO}_3$  and  $\text{InGaAs}$ , assuming a  $\text{LaAlO}_3$  film stoichiometry  $\text{La} : \text{Al} : \text{O} = 1 : 1.1 : 3.1$ . Furthermore, nearly identical Al and O profiles (Fig. 3 inset), indicate the absence of another O-containing phase at the interface. Thus, no interfacial oxide layer is observed for either as-deposited dielectrics or dielectrics after annealing to  $\leq 500^\circ\text{C}$ .

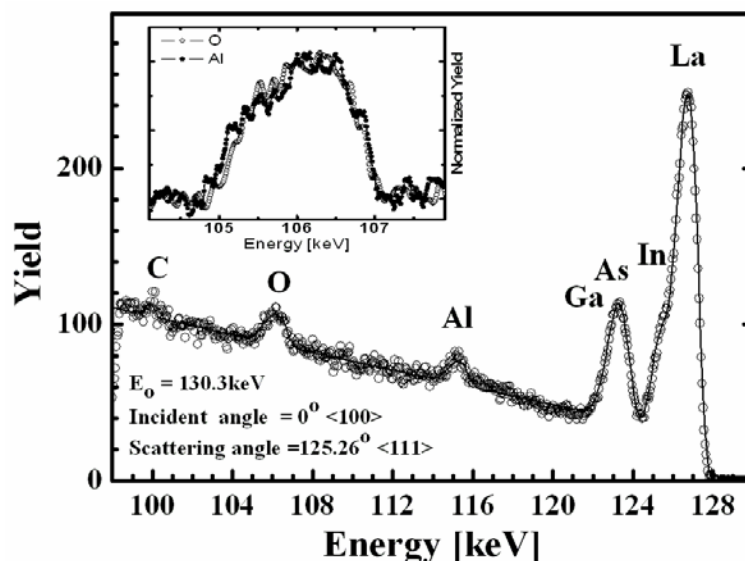


Fig. 3. An MEIS energy spectrum (circles) of a 3.6 nm-thick amorphous  $\text{LaAlO}_3$  on InGaAs. The quantitative model data (line), where an oxide-free interface is assumed, is also shown. Al and O peaks are shown in the inset (normalized, background subtracted).

#### Metallization and sulfur passivation in the Al/HfO<sub>2</sub>/S/InGaAs system

Somewhat surprising results were obtained for the S-profile in an S-passivated stack after metallization. In Fig. 4 we show MEIS spectra for an Al/HfO<sub>2</sub>/InGaAs stack.

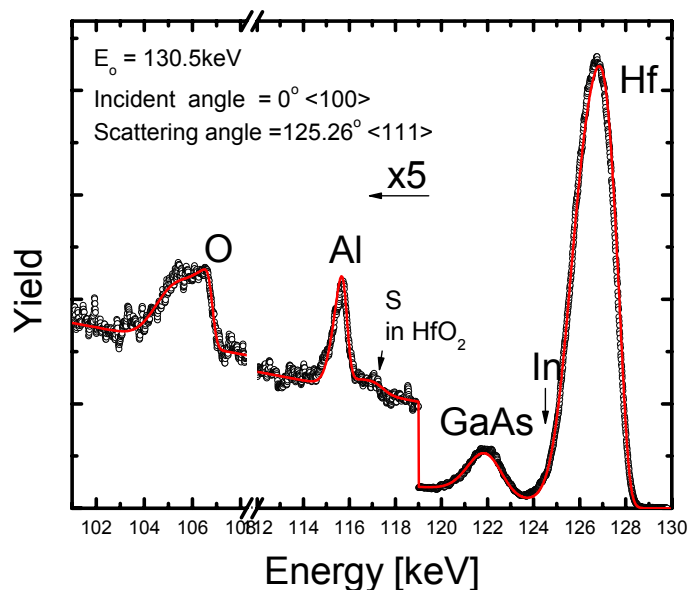


Fig. 4. MEIS spectrum of Al/HfO<sub>2</sub>/InGaAs stack. The red line through the spectrum is a fit to a model multilayer structure.

The stack modeling (to be presented in an upcoming paper) still show that S remains incorporated in the film, however upon Al metallization, the S moves up in the film close to the metal electrode (and/or incorporates into the Al at the interface) forming a sulfide or oxysulfide layer.

In Fig. 5 we present a simple schematic diagram that best captures the structure and position of the layers after metallization. Although one might assume that metallization would have no effect on S or O located 1-3 nm away in the dielectric, there was net S movement up in the film. Similar observations have been made in the past for oxygen in metal oxide dielectrics, driven by the high O affinity of some electrode metals.(10-12)

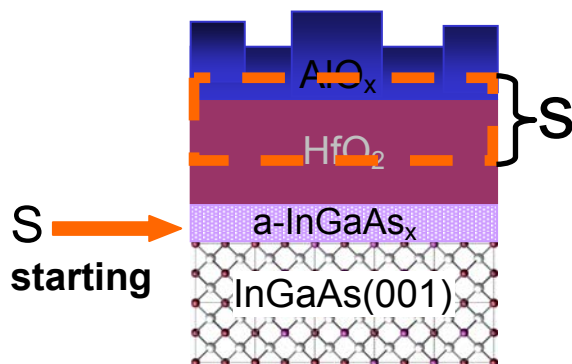


Fig. 5. Model of the Al/HfO<sub>2</sub>/InGaAs structure after metallization. Note that S, originally deposited at InGaAs/HfO<sub>2</sub> interface, is transported into and through the high-K layer.

As the sulfur backscattering signal in Fig. 4 is weak, the movement of the S atoms was confirmed by XPS and sputtering. In Fig. 6, the XPS spectra of the system prior to and after sputtering show that S is present in the Al/HfO<sub>2</sub>/InGaAs structure, and is not present by the time the Al layer is sputtered and HfO<sub>2</sub> layer is thinned to exposing the InGaAs layer. One would expect a sulfur signal increase after the Al layer is removed, if sulfur is indeed localized at HfO<sub>2</sub>/InGaAs interface, since the thickness of the layer above S-containing layer is reduced. The complete disappearance of S indicates that S was initially in the part of the structure which was removed during the sputtering.

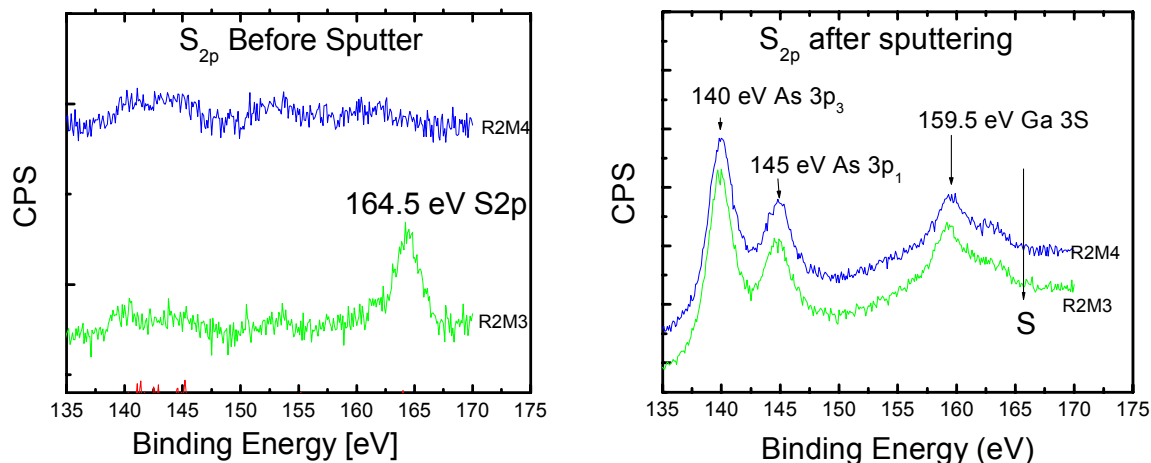


Fig. 6. XPS spectra of the As 3p, Ga 3s and S 2p region of the spectrum. Note that there is sulfur in the Al/HfO<sub>2</sub>/InGaAs structure (bottom left, green spectra), compared to the reference sample with no sulfur passivation (top left, blue curve). There is some sulfur present in the HfO<sub>2</sub> layer at a depth before the InGaAs layer is visible.

Further studies are in progress to better understand the thermal and chemical stability of these rather complex multicomponent, multilayer systems, and to correlate these results with device electrical properties.

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