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Lanthanum silicate gate dielectric stacks with subnanometer equivalent oxide thickness utilizing an interfacial silica consumption reaction

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A silicate reaction between lanthana and silica layers has been utilized to eliminate interfacial silica in metal-insulator-semiconductor devices and to obtain devices with very low equivalent oxide thickness (EOT). This provides a simple process route to interface elimination, while producing a silicate dielectric with a higher temperature stability of the amorphous phase. The La_2O_3 layers in this study are deposited by reactive evaporation on (001) Si covered by a ~0.8–1.0-nm-thick SiO_2 chemical oxide, and are capped *in situ* with a Ta gate, followed by a reaction anneal, which lowers the EOT from greater than 1.5 nm for the as-deposited bilayer stack to as low as 0.5 nm. Electron energy-loss spectroscopy and medium-energy ion scattering are used to show that a temperature of 400 °C is sufficient for the formation of the silicate gate dielectric. Gate leakage currents as low as 0.06 A/cm^2 are obtained for stacks having an EOT of 0.63 nm, orders of magnitude below that of SiO_2 having the same EOT value. Electrical breakdown is observed at applied fields above 16 MV/cm. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1988967]

I. INTRODUCTION

In the effort to scale metal-oxide-semiconductor field-effect transistor (MOSFET) devices to achieve a higher device density, it is apparent that the use of silica (SiO_2) and SiO_xN_y gate dielectrics will soon reach their practical limit. According to ITRS projections[1] within a few years MOSFETs will require a gate dielectric thickness of less than 1 nm, at which point gate leakage currents from tunneling through the thin SiO_xN_y layer would be unacceptably high.[2–4] Therefore, higher dielectric constant (high-κ) materials are being investigated to replace SiO_2, which can be made physically thicker (hence potentially lower leakage) compared with the equivalent SiO_2 thickness [equivalent oxide thickness (EOT)] needed to achieve that capacitance density. Several candidate materials are currently being investigated. A sufficiently high dielectric constant (κ), large bandgap (E_g) and band offsets relative to the conduction and valence bands of silicon, thermodynamic stability in contact with silicon, and retention of the amorphous phase at high temperatures are some of the key requirements to be met.[3,5–7] Lanthanum oxide and lanthanum silicate dielectrics are among the candidate high-κ dielectrics as they meet many of these requirements. Bulk properties for lanthana include κ ~25–30 and E_g~5.5 eV (band offset of 2.3 eV).[7] Lanthanum silicate has a lower dielectric constant, but a higher temperature stability of the amorphous phase.[3,8]

One of the greatest difficulties involved in the attempt to fabricate metal-insulator-semiconductor (MIS) devices with an EOT of less than 1 nm is the formation of an interfacial silica layer between the silicon and high-κ dielectric. These silica layers form either accidentally due to the presence of excess oxygen during deposition or are required as a nucleation layer for certain deposition processes such as atomic layer deposition. For example, to minimize interfacial SiO_2 growth and achieve and EOT value below 1 nm for Hf-based dielectrics, processing steps such as codepositing hafnium and silicon without oxygen and annealing in a nitrogen-rich atmosphere to obtain an oxynitride dielectric are utilized.[9] In contrast with the Hf-based dielectrics, rare-earth-based oxides (such as lanthana) have a large driving force to react with silica to form silicates.[10] It has previously been shown that a lanthana dielectric will react with an underlying silica layer to form a silicate,[11–14] and that lanthanum silicate is less reactive than lanthana with substrate silicon, and atmospheric gases such as O_2 and H_2O.[14–16] Although it has been observed that the deposition of La directly on Si, with post oxidation to form La_2O_3, results in very nonuniform films;[16] an EOT as low as 0.50 nm has been reported for a La_2O_3 gate dielectric with an Al gate,[15] while an EOT of 0.75 nm has been reported for lanthanum silicate using a gold gate.[16] Silicate films are believed to be more stable with respect to reaction with silicon and ambient air, but their inherently lower dielectric constants have made it difficult to achieve EOT values as low as those reported for their pure metal-oxide counterparts.

The elimination of interface SiO_2 for high-κ oxide dielectrics on silicon has been studied by a number of research

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groups, and has been achieved using different approaches for different oxide systems. For example, lanthanum aluminate has been deposited on Si at 100 °C with no interface SiO_2 by starting with a clean (001) Si surface by thermally desorbing native SiO_2.[17] HfO_2 has been deposited on Si without interfacial SiO_2 by a decomposition reaction of the native SiO_2 during growth at elevated temperatures.[18] Other reports utilizing a silicate reaction, such as the case of Y_2O_3 on silicon,[19] required temperatures in excess of 900 °C for the reaction to go to completion. In the present study, we show that to consume interfacial SiO_2 forming a lanthanum silicate (a) a temperature as low as 400 °C is sufficient and (b) this is indeed a pathway to achieve lower EOT for MIS devices.

We show below that the lanthana-silica reaction can be used as an effective way to produce gate stacks with an EOT as low 0.5 nm by designing the layer thicknesses such that the interface silica is completely consumed in the silicate reaction. In addition this reaction is found to enhance film uniformity. The elimination of the silica interface is conclusively demonstrated by high-angle annular dark-field (HAADF) imaging in scanning transmission electron microscopy (STEM) in combination with electron energy-loss spectroscopy (EELS), and by medium-energy ion-scattering (MEIS) spectroscopy. Here we focus only on low-temperature processing of the gate stacks.

II. EXPERIMENT

Lanthana-based gate dielectrics have been deposited using reactive evaporation in an ultrahigh vacuum (UHV) molecular beam epitaxy (MBE) system designed for processing 8-in. wafers. Substrates used in this study were 6-in. *n*-type (001) Si substrates (Sb-doped, 0.02 Ω cm). All substrates were RCA-cleaned using the sequence SC1 (using a mixture of 5 H_2O:1 NH_4OH:1 H_2O_2 for 5 min at 75 °C), buffed oxide etch (~5-s dip), and SC2 (using a mixture of 5 H_2O:1 HCl:1 H_2O_2 for 5 min at 75 °C). This left a thin chemical oxide on the surface, as verified by reflection high-energy electron diffraction (RHEED) showing an approximately amorphous substrate surface before growth. The thickness of the chemical oxide was about 0.8–1.0 nm.

The lanthana dielectric layer was deposited using reactive evaporation. Elemental La was thermally evaporated (in a tungsten crucible) using a high-temperature effusion cell, while oxygen gas was introduced into the chamber via a mass-flow controller. The film growth rate was ~0.2 nm/min in an oxygen pressure of 4×10^{-7} Torr. Substrate rotation during growth was used to optimize uniformity, and the wafer was kept at a low temperature (<200 °C) to promote a smooth, continuous amorphous film with minimal interfacial reaction. Film thickness was measured using a calibrated quartz crystal microbalance. Due to the propensity of lanthana to form hydroxides and carbonates upon air exposure,[20] we capped the films *in situ* with *e*-beam-evaporated tantalum (~60 nm). Tantalum has several properties making it useful as a gate electrode: a high melting point, thermodynamic stability in contact with lanthana,[21] a suitable work function for *n*-type metal-oxide semiconductor (NMOS) devices (~4.2 eV),[22] and relative ease of selective etching using plasma processing.

Upon removal from the MBE system, a dc-magnetron-sputtered tungsten electrode was added (on top of Ta, and on the back of the Si wafer) to aid the formation of a good electrical contact with MIS devices after post-processing treatments. To examine the conditions for complete silica consumption, post-process rapid thermal anneals (RTA) of the La_2O_3/SiO_2 gate dielectric stacks were performed in flowing nitrogen. Some films have undergone *in situ* reaction anneals before the Ta gate deposition, typically at 500 °C for 10 min in 5×10^{-7}-Torr O_2, to control the O_2 pressure during the anneal and to eliminate the chance for reaction with the Ta gate. Contact areas were defined using standard photolithographic processing, followed by reactive ion etching (RIE) of the W/Ta gate electrode layers in a SF_6/O_2 mixture.[23]

After the RIE process, some devices were subjected to forming gas anneals in a quartz tube vacuum furnace using 1% H_2 in N_2 at 400 Torr total pressure. Electrical testing of capacitance and gate leakage characteristics has been performed using HP 4192A impedance analyzer and HP 4145A semiconductor parameter analyzer probe stations. Device parameters such as the EOT and flatband voltage (V_{fb}) have been extracted from the *CV* data using the NCSU CVC modeling program.[24] All electrical results were obtained from either 50×50-μm^2 or 71×71-μm^2 square capacitor areas and measured at 1 MHz.

Transmission electron microscopy (TEM) cross-section samples were prepared by standard sample preparation techniques, with ion milling using 3.3-kV Ar ions as the final step. High-resolution TEM (HRTEM) was performed using a field-emission TEM (Tecnai F30 U-TWIN, Cs=0.52 mm) operated at 300 kV. HAADF imaging and EELS in STEM were performed using a field-emission TEM (Tecnai F20 S-TWIN) equipped with a Gatan imaging filter (GIF) and operated at 200 kV. EELS spectra were obtained using a 2-mm GIF entrance aperture and a 0.5-eV/ch dispersion to include both O *K*-edge (532 eV) and La $M_{4,5}$-edges (at 849 and 832 eV, respectively). The probe size for EELS was estimated to be ~3.5 Å from the resolution in the HAADF images. The energy resolution was 1.5–1.7 eV (full width at half maximum of the zero-loss peak). Each spectrum was acquired for 15 s to obtain a sufficient signal-to-noise ratio, and specimen drift was about 5 Å during this time, further reducing the spatial resolution. After appropriate background subtraction, chemical profiles were generated from spectral counts by integration over suitable energy ranges. Such profiles showed qualitative changes in the concentration of a given element along the profiled line and did not represent true relative elemental concentrations.

The MEIS experiments were performed using 130.8-keV H^+ beams using a double alignment geometry in the (110) scattering plane, in which the incoming beam is aligned with the Si [100] channeling direction and the detector axis is aligned with the $[\bar{1}11]$ crystallographic axis. Such scattering geometries are very useful for reducing backscattered background signal from bulk Si and allow a detailed study of the otherwise weak O signal. Backscattered ion energies were analyzed with a high-energy-resolution toroidal electrostatic

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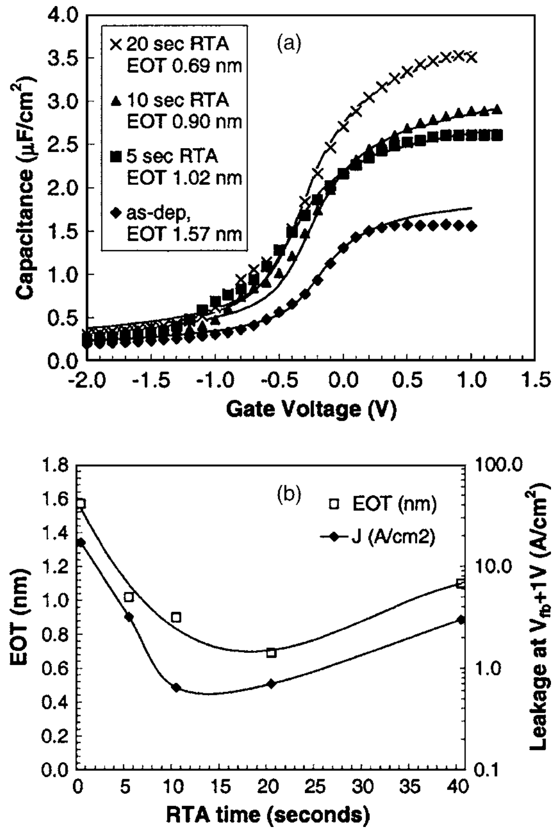

FIG. 1. (a) *CV* curves showing the effect of gate stack RTA time at 400 °C in N_2; the dots represent measured data and the lines modeled fits. (b) Corresponding plot of EOT (nm) and gate leakage $J(\mathrm{A/cm^2})$ at $V_{fb}+1\mathrm{V}$ for the same devices. Dielectric reactions are evident from the changing stack EOT and J with RTA time. Capacitors are 71×71 μm^2, measured at 1 MHz.

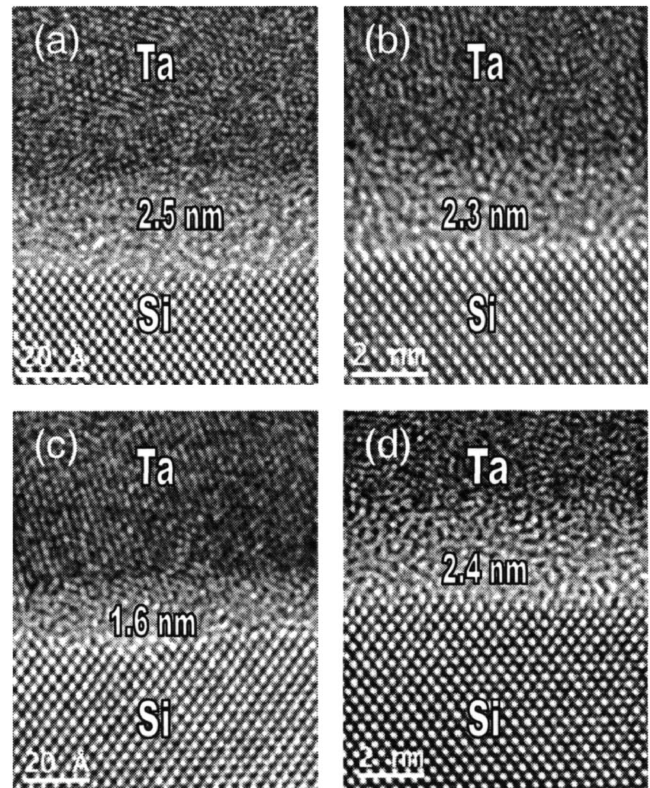

FIG. 2. TEM cross sections showing (a) as-deposited $Ta/La_2O_3/SiO_2/Si$ gate stack and after reaction anneal of gate stacks at 400 °C in N_2 for (b) 10, (c) 20, and (d) 40 s. The amorphous dielectric thickness is indicated in each image.

ion detector ($\Delta E/E\sim0.1\%$).[25,26] Depth profiles of the elements were obtained from simulations of the backscattered ion energy distribution (with the assumption that film densities are known or can be extrapolated from films of known composition). Quantitative depth profiles for different species can be extracted with a resolution as high as 3 Å in the near-surface region. However, the depth resolution deteriorates for deeper layers[26] due to the statistical nature of the ion-solid interaction. The samples analyzed by MEIS were reacted to form a silicate in the MBE growth chamber at 500 °C for 10 min in 5×10^{-7}-Torr O_2 without any metal gate capping to enhance the resolution of the dielectric layer. Thus, these films have been exposed to air for a number of days before the MEIS measurement. The film thickness and composition are obtained by fitting the measured MEIS spectra to theoretical simulations.

III. RESULTS AND DISCUSSION

A. Examination of the La_2O_3/SiO_2 reaction

MIS devices employing lanthana/silica bilayers show a clear reduction in EOT after being subjected to RTA treatments of varying times, as is evident from the *CV* curves of Fig. 1(a). During RTAs in N_2 at 400 °C for times up to 40 s, the EOT of W/Ta/1.1-nm $La_2O_3/\sim0.8$–1.0-nm SiO_2/Si MIS devices decreases from 1.57 nm for the as-deposited stack to a minimum of 0.69 nm after 20 s. In Fig. 1(b) the EOT and gate leakage (J) at 1.0 V above the flatband voltage ($V_{fb}+1$ V) are plotted as a function of the RTA time. Note that the minimum EOT correlates with the minimum leakage after roughly a 20-s anneal time for these stacks. Longer anneals (40 s or more) result in undesirable increases in the EOT and leakage current density. The fact that the EOT reduces to 0.69 nm for a gate stack with initially ~0.8–1.0 nm of SiO_2 implies that the silica layer has changed as a result of the RTA treatment.

Identical dielectric stacks (pieces from the same wafer, but without the W contact layers) were analyzed by HRTEM and STEM (EELS and HAADF). Figure 2 shows HRTEM images of (a) the as-fabricated gate stack and gate stacks after 400 °C RTA treatments in N_2 for times of (b) 10, (c) 20, and (d) 40 s. The reduction of the total amorphous dielectric physical thickness from 2.5 nm for the as-deposited stack to 1.6 nm after the 20-s RTA indicates that annealing results in film densification, and all measured thickness changes are in general agreement with the measured EOT values shown in Fig. 1. The change in gate dielectric thickness due to the RTA treatment (for up to 20-s times) could be due to both (1) reaction processes resulting in a high-density product phase and (2) a densification of the low-density La_2O_3 deposited at ambient temperature.[27] Thinning of the amorphous layer would also occur if the SiO_2 at the interface decomposed by reduction to Si (giving up oxygen to the deposited dielectric or the gas phase). This mechanism has been observed for some dielectrics deposited on SiO_2 at higher temperatures,[19] and cannot be excluded as a possibility based on the HRTEM

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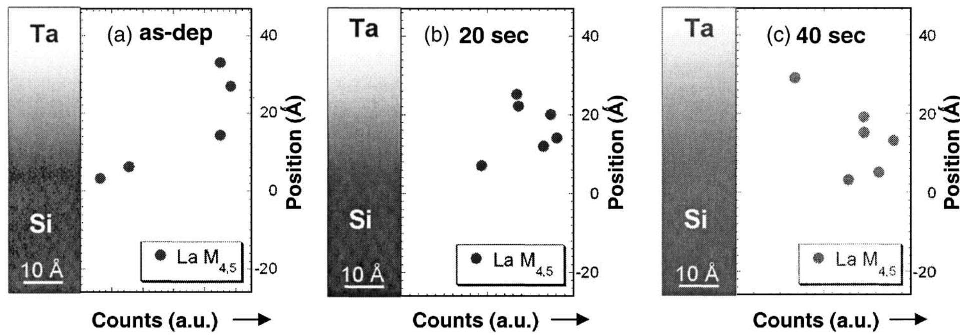

FIG. 3. HAADF images and corresponding La $M4$, 5-edge intensity (counts increasing to the right) measured from background-subtracted EELS spectra, with position indicated as distance away from the Si interface (taken as zero). The figures show gate stacks (a) as-deposited, (b) after a 20-s RTA, and (c) after a 40-s RTA in N_2.

images alone, but is not expected.[12] The thickness increase observed after the 40-s RTA indicates that an additional reaction process occurs, to be discussed later. Comparing the measured physical thickness of the gate dielectric and the electrically measured EOT, a dielectric constant of ~ 10 is obtained. This indicates a silica-rich reaction product (having more silica than the $La_2Si_2O_7$ diorthosilicate composition), applying a simple mixing rule for the silicate dielectric constant from the lanthana ($\kappa \sim 28$) and silica ($\kappa = 3.9$) components. Alternatively, the relatively low dielectric constant may also be explained with a graded silicate composition, with some lower-k, silica-rich material connected in series with a lanthana-rich dielectric.

To obtain compositional information of the dielectric layer, EELS in STEM as well as MEIS have been utilized. The La peak intensity obtained from EELS line profiles of microprobe spots across the dielectric thickness for the as-deposited gate stack and for the gate stack after 20- and 40-s RTAs at 400 °C in N_2 are shown in Figs. 3(a)–3(c). Figures 3(a)–3(c) also include the corresponding HAADF images on the left side. The intensity of the La EELS peak increases with distance away from the HAADF image (to the right), and the stack thickness scale is shown on the right with the silicon surface taken as the zero position. The difference between the dielectric thickness values obtained by HRTEM (Fig. 2) and HAADF can be explained as instrument effects and/or sample preparation effects.[28] Regions of intermediate brightness in the HAADF image correspond to the amorphous dielectric. The dielectric layer and Ta gate appear brighter than the Si substrate due to atomic number sensitivity of these images. An interfacial SiO_2 layer would be visible as a dark layer at the substrate interface and is visible in the as-deposited sample shown in Fig. 3(a) and the sample annealed for 10 s (not shown). In contrast, no such layer is visible in Figs. 3(b) and 3(c), indicating elimination of the interfacial SiO_2 after the 20-s RTA at 400 °C. EELS shows that La is detected immediately adjacent to the Si interface for the 20- and 40-s annealed stack, albeit with some gradient for the 20-s RTA case. In contrast with the as-deposited and 20-s annealed stacks, a slight drop in La concentration is observed near the Ta interface after a 40-s anneal, indicating possible intermixing/reaction between the La-silicate layer and Ta, or roughening of this interface. Ta is predicted to be stable in contact with La_2O_3. However, Ta is not stable in contact with SiO_2,[29] thus it may not be stable in contact with the silicate. The stability of Ta in contact with a La-silicate will thus require further study.

Additional compositional profiling was obtained using MEIS. Analysis of a similar (but not W or Ta capped) SiO_2/La_2O_3 bilayer, after an *in situ* reaction anneal at 500 °C for 10 min in 5×10^{-7}-Torr O_2, is shown in Fig. 4. An MEIS spectra can be fitted with a dielectric layer consisting of a 1.2-nm $(La_2O_3)(4\ SiO_2)$ film.[30] No interfacial SiO_2 is observed within the spatial resolution and detection limit of the technique as can be seen from a comparison of the La and O peak areas. This applies even though these films have been exposed to air for a couple of days. In agreement with the electrically measured EOT and HRTEM images that indicate a relatively low dielectric constant (~ 10), the composition obtained by MEIS is silica-rich and thus consistent with this dielectric constant. The thickness observed by MEIS is less than that obtained by HRTEM, probably due to differences in film density values for the MEIS simulation and the actual film.

B. Utilizing this silicate reaction to minimize the EOT of MIS devices

The annealing study of the bilayer lanthana/silica gate stacks and the results in Figs. 1–4 demonstrate the effects of the silicate reaction on the electrical properties and on the potential to use this reaction to eliminate interfacial silica and obtain subnanometer EOT MIS devices. Due to the degradation of the electrical properties after a 40-s RTA, and the

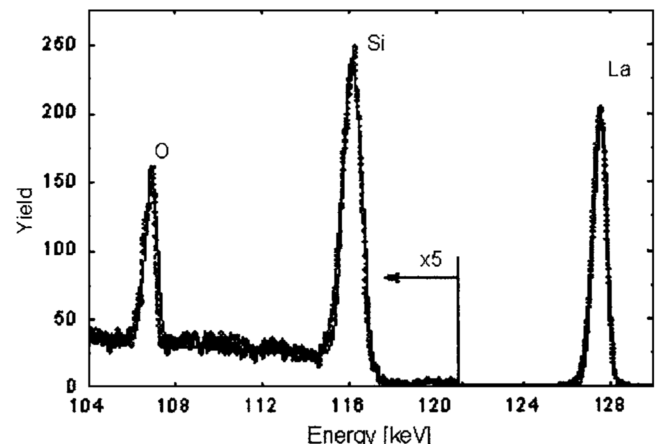

FIG. 4. MEIS (130.8-keV H^+) spectrum of a $La_2O_3/SiO_2/Si$ stack after an *in situ* reaction anneal at 500 °C for 10 min in 5×10^{-7}-Torr O_2. A MEIS simulation (solid line) fit to the data indicates a single silicate layer of 12A $(La_2O_3)(4\ SiO_2)$ and no detectable SiO_2 at the interface.

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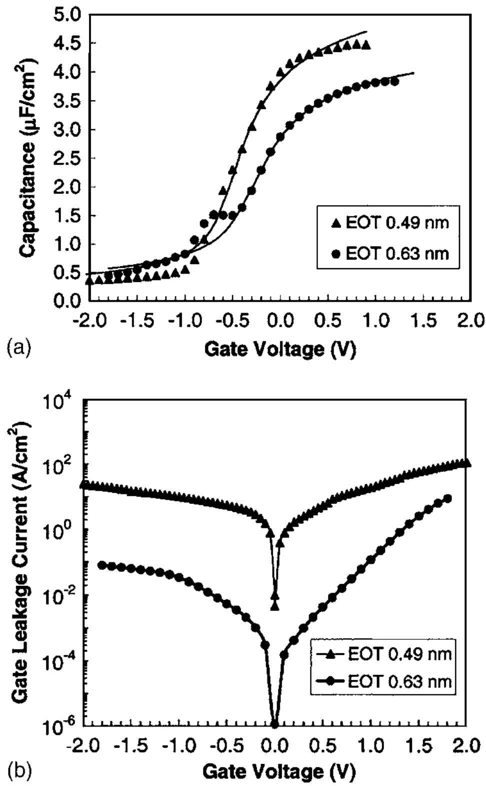

FIG. 5. (a) *CV* curves and (b) *I–V* gate leakage of *in situ* reaction annealed MOS devices having EOT values of 0.49 and 0.63 nm, and corresponding leakage at $V_{fb}+1V$ of 5×10^{0} and 6×10^{-2} A/cm^2, respectively. The dots represent the measured data, while the lines in (a) are fits using the CVC model. Capacitor size is 50×50 μm^2, using a 1-MHz measurement frequency.

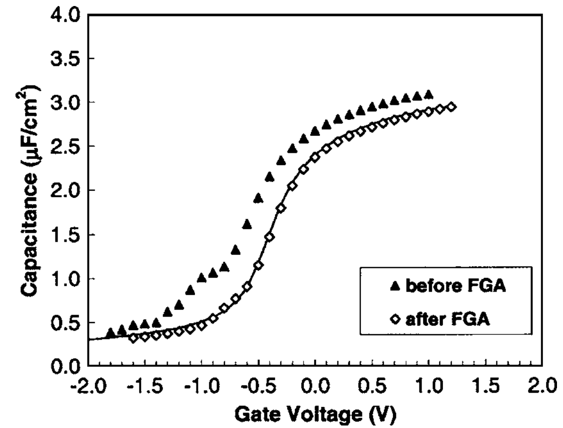

FIG. 6. Effects of a 400 °C, 20-min forming gas anneal on a lanthanum silicate dielectric stack; the data points show positive and negative *V* sweeps, the line a modeled fit (EOT 0.89 nm) to the data. The flatband voltage has shifted 0.23 V closer to the expected value (a reduction in positive charge density), and the "hump" related to the interface traps has been reduced. Capacitors are 50×50 μm^2, measured at 1 MHz.

EELS observation that Ta may interact with the silicate layer, we have varied the annealing processes in an attempt to further minimize EOT. By *in situ* processing of the dielectric bilayer *before* depositing Ta, better stability of the gate stack during processing and lower EOT and lower leakage currents are obtained. For example, La_2O_3/SiO_2 bilayers deposited using the same deposition conditions but *in situ* annealed at 600 °C for 10 min (~30 °C/min ramp rates) in 5×10^{-7} Torr O_2 with subsequent *in situ* Ta gate deposition show lower EOT values (0.63 nm) and lower leakage (0.06 A/cm^2) [Figs. 5(a) and 5(b)]. *I–V* curves measured at high voltages show that breakdown occurs at fields above ~16 MV/cm. Using a 500 °C *in situ* reaction anneal, an EOT of 0.49 nm was obtained for a Ta-gated MIS device, also shown in the curves in Fig. 5. Although leakage values are highest for these thin devices [leakage at $(V_{fb}+1\ V)=5\times10^{0}$ A/cm^2] and they are very sensitive to further post processing, such a low EOT value is promising.

Thus, a lower EOT can be obtained by annealing without the presence of the Ta gate metal, and the EOT remains low after a longer anneal time (10 min as opposed to 40 s). This would indicate that, during RTAs with the blanket (unetched) Ta gate metal covering the unreacted dielectric bilayer, the Ta is interacting with the dielectric during heating and/or that O_2 in the N_2 RTA ambient or dissolved oxygen in the Ta gate provides an oxygen source (since the amorphous dielectric thickness increases). Recently it has been concluded that dissolved oxygen in W can result in interface SiO_2 growth of up to 2.0 nm;[31] thus a similar effect may be occurring for the case of W/Ta and Ta gates as used here.

A 400-Torr forming gas anneal (FGA) of 400 °C for 20 min can effectively lower interface trap density and bulk charge, as shown in Fig. 6. The FGA reduces the hump in the *CV* curve attributed to interface traps,[32] reduces hysteresis in the *CV* curves, and shifts V_{fb} closer to the ideal value for these MIS devices with Ta gates. However, for many samples we examined, a higher-temperature FGA anneal was not effective in eliminating the "hump" due to interface traps, and the flatband shift due to positive fixed charge was significant. Further study is ongoing in the area of interface and bulk defect characterization for thin lanthanum silicate films and the conditions required to minimize and passivate them. A simulation model which allows us to determine defect energy distributions, and trapping/detrapping time constants, is currently being evaluated.[33]

IV. SUMMARY

Interface SiO_2 can be consumed by a reaction with lanthanum oxide to form a silicate. We show that (a) a temperature as low as 400 °C is sufficient to consume an interfacial SiO_2 layer of 0.8–1.0-nm thickness, and (b) that this reaction is a viable pathway to achieve EOTs below 1.0 nm for MIS devices. Lanthana-based gate stacks with EOT values as low as 0.5 nm have been fabricated utilizing this approach. Within the limits of high-resolution STEM/EELS analysis, and MEIS, we show that the interface silica can be completely eliminated through proper choice of time and temperature processing conditions, producing a silicate dielectric. Devices with an EOT of 0.63 nm have leakage currents of 0.06 A/cm^2, breakdown fields above 16 MV/cm, and an effective dielectric constant ~10.

The lowest EOT values are achieved by an *in situ* reaction anneal before depositing an *in situ* Ta gate. This indicates that issues such as oxygen pressure control and reaction with the gate metal are important issues to be dealt with

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when considering gate stack stability. Our ongoing research includes studying the high-temperature stability of these gate stacks and minimizing the density of interface state traps. These questions must both be resolved for this dielectric to satisfy current MOSFET process requirements.

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