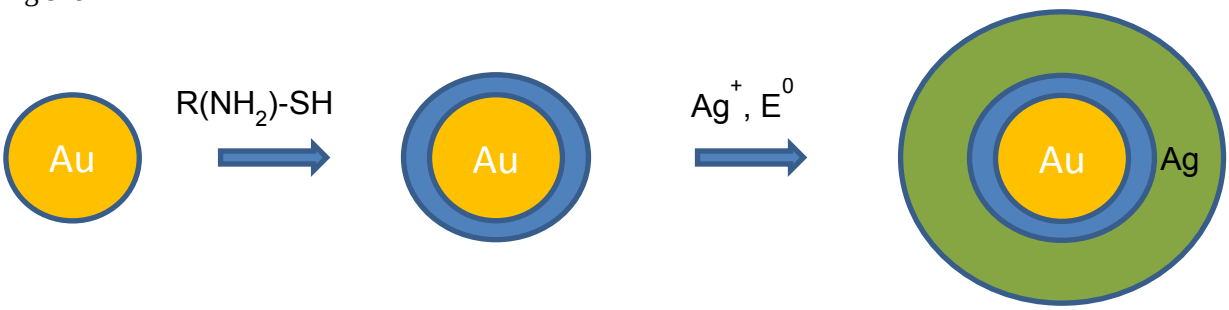
P9826B, Winter 2013

Presentation #2 topics

Case Study #1

Smith and co-workers used selective adsorption and electrochemistry to build core-shell structures with gold nanoparticles (Au-NP). They started with ~ 5nm in diameter Au nanoparticles, functionalized them with thiol molecules ($R(NH_2)$-SH, $R=C_{10}$-C_{14}) followed by reduction in Ag^+ solution to form continuous Ag shell



Assuming that both thiol-covered Au-NP and Ag-thiol-Ag core-shell particles can be deposited on the surface by spin coating, suggest a set of surface sensitive characterization techniques

(1) to prove that core-shell system was formed;

(2) to estimate the thickness of Ag layer.

Justify your selection.

Case Study #2

Postdoctoral fellow Bob oxidizes Al film (~ 1μm thick) deposited on top 10μm ITO film/glass substrate for optical sensor applications.

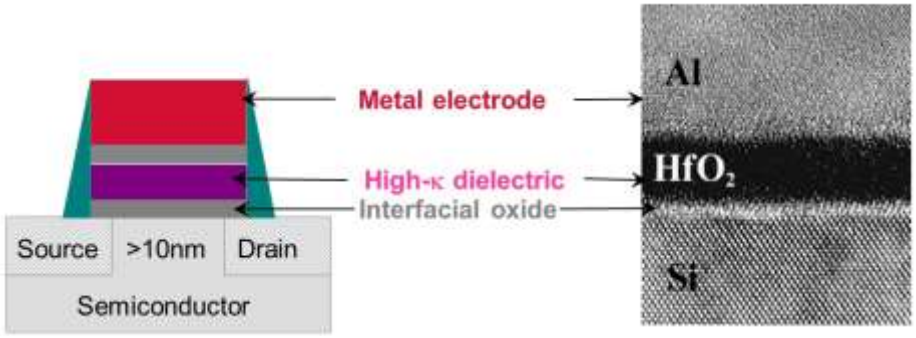
First he tries Al oxidation in oxygen (O_2) at high temperature (~300^{o}C), than he decides to compare it with electrochemical oxidation in solution of H_2SO_4.

(1) Propose several (at least 3) methods to compare oxidation rate in oxygen to the electrochemical one.

(2) What oxidation route is referable, assuming that Al_2O_3 layer at least 200nm thick need to be produced? Comment on the morphology/structure of these Al_2O_3 layers.

Case Study #3

Silicon dioxide was used as a gate oxide material for the last four decades because of its manufacturability an ability to deliver continued transistor performance improvement as it has been made ever thinner. Over the last few years SiO_2 has been replaced first by SiON, then by HfSiON thin films as of 2007. One potential issue with implementation of Hf-based dielectic films is formation of "interfacial oxide", typically SiO_2, at the high-k dielectric/Si interface (see diagram and representative high-resolution transmission electron microscopy image below)



Several different metal electrode materials were introduced instead of previously used heavily-doped silicon. Imagine that you examine several material metal candidates, such as Sc, Ti, Al and Ta, to introduce them into transistor structure. However additional interface layer was also observed at the metal/HfO_2 interface, as indicated by the grey layer between metal electrode and high-k dielectric on the diagram above).

(a) Propose two different ways to examine 10nm metal/3nm HfO_2/Si (001) substrate and learn composition of interface layers between HfO_2 and Si, and HfO_2 and metal.

(b) Based on their (1) stability in air; (2) thermodynamic stability next to HfO_2; (c) stability to stay in an amorphous state, rank these four metals as potential candidates for metal electrodes.

Case study #4

Since the discovery of graphene, researchers have continued to examine its unique properties and are working to integrate it in a wide array of applications and potential products. Several other compound materials, such as BN, silicene, and MoS_2, are new star materials, as they are thought to have similar electronic properties to graphene but ought to be more compatible various components in silicon-based electronic devices.

MoS_2 was used extensively in the past as a lubricant, hydrodesulfurazation catalyst, as well as a catalyst the formation of alcohols from syngas. Mechanical exfoliation allows access to single layer and few layer MoS_2 films. As an alternate route, MoS_2 layers can be grown epitaxially on various metal and semiconductor substrates.

(a) In your research project you need to find a suitable single-crystal substrate surface to grow MoS_2 epitaxially. If you have several substrates, including Ru(111), Ni(001), Cu(111), Ag(110), Au(111), sapphire (0001), which one would you choose? Explain your selection. What deposition method do you choose for the growth?

(b) How can you characterize MoS_2/metal substrate system for establish (i) formation single or multiple layer formation; (ii) MoS_2 stoichiometry; (iii) absence of contaminations?

Case study #5

In late 90s, IBM and other semiconductor industries introduced the concept of SOI (silicon on insulator) technology with which a silicon wafer is converted to the structure of crystalline Si / SiO_2 / silicon wafer. The top two layers are both about 200nm. With the SOI wafer, one can then fabricate microelectronics on the top crystalline Si layer and all devices are electrically isolated such that the parasitic device capacitance is drastically reduced and the switching frequency can be raised. Since then, a niche industry has been created in producing such SOI wafers.

The way to make SOI wafers is to implant O^+ (or O^{2+}) ions into a silicon wafer with high enough energy that most oxygen projectiles can penetrate to 250nm or so. One can then anneal the sample after implantation (post-implanation crystallization) or implant at high temperature (dynamic regrowth) to form the crystalline Si layer with an oxide beneath it.

(a) Use SRIM to find the ion energy requirement for an O^+ ion penetration range of about 250nm. Use your sputter-yield result to show that your SOI process is practical. What methods would you use to confirm that you achieved proper SOI structure.

(b) In SIMS, we can use oxygen ions as primary ions to produce secondary ions. In fact, this is the common way to detect trace amount of boron in silicon. If the sputter yield of boron and silicon are the same and their ionization yields are both 0.1, comment on whether you should use your ion energy for the SOI technology to do SIMS studies of boron in silicon, or you should lower down the ion energy to below certain threshold energy.